What is claimed is:

1. A semiconductor memory device comprising:

a redundant memory cell for use instead of a memory cell when the memory cell has a defect;

an electrode applied with a test signal for setting a test condition from outside in testing the redundant memory cell; and

an output circuit for outputting data read out of the memory cell and the redundant memory cell,

wherein when the test signal is applied to the electrode to set the test condition for the redundant memory cell, the output circuit is configured to output data read out of the redundant memory cell at a level different from a signal level of data read out of the memory cell for output.

2. A semiconductor memory device according to claim 1, wherein when the test condition for the redundant memory cell is set, the output circuit outputs the data read out of the redundant memory cell of high-level potential at a lower potential than a predetermined voltage.

3. A semiconductor memory device according to claim 1, wherein when the test condition for the redundant memory cell is set, the output circuit inverts and outputs data read out of the redundant memory cell.

4. The semiconductor memory device according to claim 1, wherein the output circuit comprises:

a first logic gate for determining that both the test signal and an internal control signal created based on the test signal have normal logical values; and

a second logic gate for inverting and outputting the data read out of the redundant memory cell based on an output signal of the first logic gate.

5. A semiconductor memory device comprising:

first and second redundant memory cells for use instead of a memory cell when the memory cell has a defect;

first and second electrodes applied with a test signal for setting a test condition from outside in testing the first and second redundant memory cells; and

an output circuit for outputting data read out of the memory cell and the first and second redundant memory cells,

wherein when the test signal is applied to both the first and second electrodes to set the test condition for the first and second redundant memory cells, the output circuit is configured to output a signal at a fixed level.

6. The semiconductor memory device according to claim 5, wherein when the test condition for the first and second redundant memory cells is set, the output circuit outputs a signal at high level or low level.

7. The semiconductor memory device according to claim 5, wherein the output circuit comprises:

a first logic gate for determining that the test signal

for the first and second redundant memory cells and an internal control signal created based on the test signal have all normal logical values; and

a second logic gate for fixing an output signal at high level or low level by an output signal of the first logic gate when a normal test condition is set.

8. A semiconductor memory device comprising:

a redundant memory cell for use instead of a memory cell when the memory cell has a defect;

an electrode applied with a test signal for setting a test condition from outside in testing the redundant memory cell; and

an output circuit for outputting data read out of the memory cell and the redundant memory cell,

wherein when the test signal is applied to the electrode to set the test condition for the redundant memory cell, the output circuit is configured to output data read out of the redundant memory cell at timing different from timing to output data read out of the memory cell.